WHAT IS CLAIMED IS:

1. A synchronous SRAM-compatible memory device having a DRAM memory array including a plurality of DRAM cells arranged in a matrix form defined by rows and columns, and operating in synchronization with a reference clock signal, the synchronous SRAM-compatible memory device comprising:

a data input/output unit for controlling input and output of data to and from the DRAM memory array;

a state control unit for controlling an operation of accessing the DRAM memory array and an operation of the data input/output unit, the state control unit receiving a chip enable signal externally provided to enable the synchronous SRAM-compatible memory device;

a refresh timer for generating a refresh request signal activated at regular intervals;

a clock period modulating unit for providing a pre-control signal to activate a non-executed refresh request signal, the pre-control signal having a logic state transition in response to every n-th clock pulse of the reference clock signal generated during an inactivation interval of the chip enable signal; and

a refresh control unit for generating a refresh control signal to control a refresh operation for the DRAM memory array, the refresh control signal being activated in response to the logic state transition of the pre-control signal.

2. The synchronous SRAM-compatible memory device as set forth in claim 1, wherein the refresh control signal is activated in response to a refresh clock signal having a period that is "n" (n is a natural number) times a period of the reference clock signal.

3. The synchronous SRAM-compatible memory device as set forth in claim 2, wherein the period of the refresh clock signal is 1/m (m is a natural number) of an inactivation interval of the chip enable signal.

4. The synchronous SRAM-compatible memory device as set forth in claim 3, wherein the "n" is a natural number equal to or greater than "2".

5. The synchronous SRAM-compatible memory device as set forth in claim 4, wherein the clock period modulating unit comprises:

clock period modulator for providing the refresh clock signal to be enabled in response to an inactivated chip enable signal and to be extended "n" times the reference clock signal; and

a flip-flop for receiving the refresh request signal as a signal input and the refresh clock

signal as a clock input.

6. The synchronous SRAM-compatible memory device as set forth in claim 2, wherein the "n" is a natural number equal to or greater than "2".

7. The synchronous SRAM-compatible memory device as set forth in claim 6, wherein the clock period modulating unit comprises:

clock period modulator for providing the refresh clock signal to be enabled in response to an inactivated chip enable signal and to be extended n times the reference clock signal; and

a flip-flop for receiving the refresh request signal as a signal input, and the refresh clock signal as a clock input.

8. The synchronous SRAM-compatible memory device as set forth in claim 1, further including:

a burst address generating unit for generating a burst address in response to a burst address enable signal from the state control unit;

a column control signal generating unit for generating a column control signal that is activated in a burst access operation; and

a column address latch for latching one of a column address externally provided and the burst address from the burst address generating unit in response to the column control signal.

9. The synchronous SRAM-compatible memory device as set forth in claim 1, further including:

a refresh address generating unit for generating a refresh address specifying a row of the DRAM memory array in response to the refresh control signal;

a row control signal generating unit for generating a row control signal in response to a row activation signal provided from the state control unit and the refresh control signal provided from the refresh control unit; and

a row address latch for latching one of a row address externally provided and the refresh address from the refresh address generating unit in response to the row control signal.

10. The synchronous SRAM-compatible memory device as set forth in claim 9, wherein the refresh control signal is activated to perform a refresh operation when the row activation signal is inactive.